Exhibit 2

U.S. Patent No. 8,549,339 ("'339 Patent")

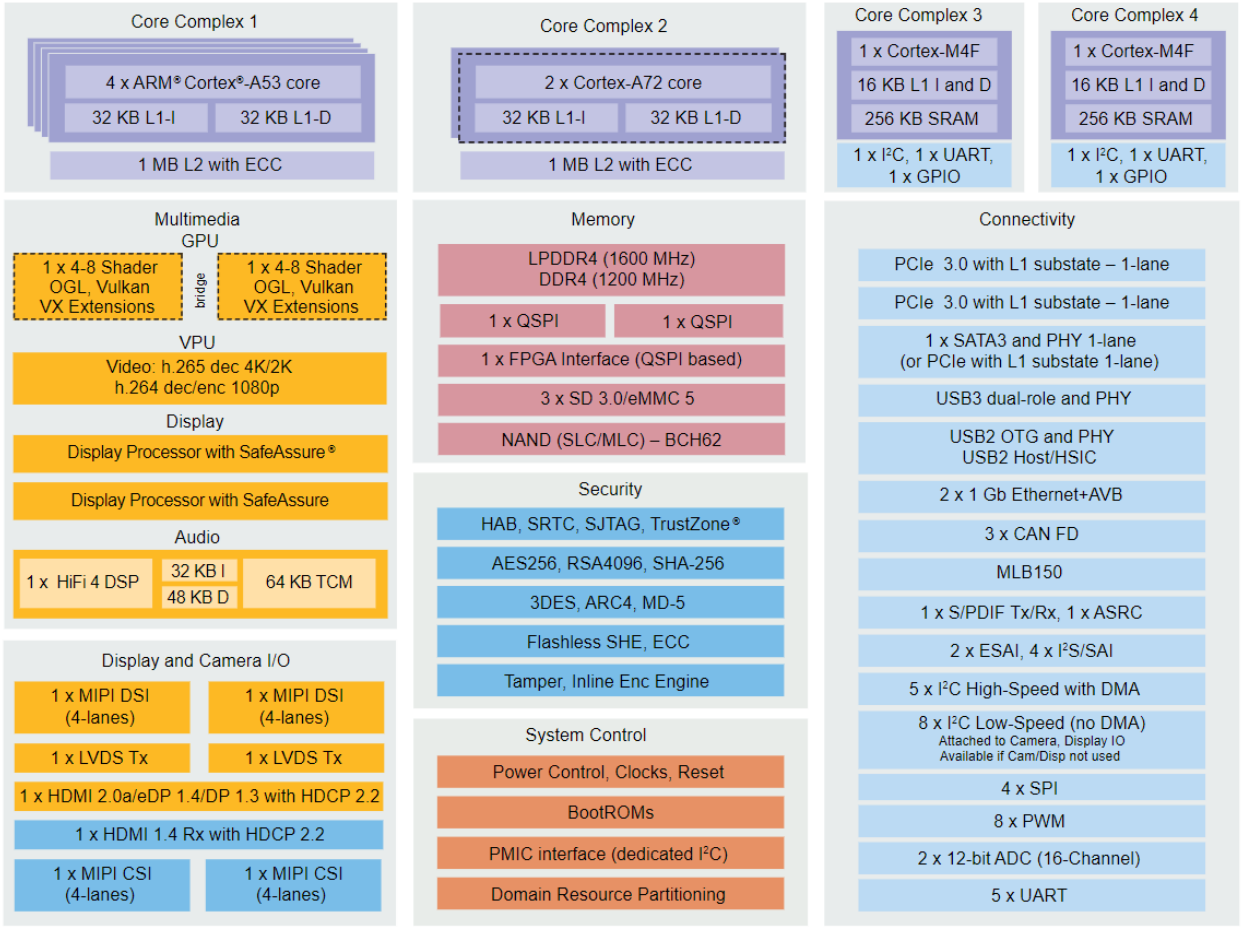
Accused Products

NXP's products comprising two or more sets of processors supporting or based on the ARM big.LITTLE architecture, including without limitation the NXP i.MX 8 Family Application Processors.

Claim 1

Claim 1	Accused Products
1. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. For example, the NXP i.MX 8 Family Application Processor contains six cores implementing the ARM big.LITTLE architecture. *See, e.g.*:

Claim 1	Accused Products



https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-applications-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8

Claim 1	Accused Products
	Features **Processor Complex** • Core Complex #1: 4x Cortex-A53 • Core Complex #2: 2x Cortex-A72 • 2x Cortex-M4F • 1x HIFI4 DSP https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-applications-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8 **1.2 Document scope** This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC. • Cortex®-A7. • Cortex®-A15. • Cortex®-A17. • Cortex®-A53. • Cortex®-A57. • Cortex®-A72. • Cortex®-A73. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	2.1 ARM® big.LITTLE™ system example A big.LITTLE system uses two different types of cores that are combined in a coherent system. big cores are designed for high performance while LITTLE cores are designed for high energy efficiency. The big cores are used for resource-intensive software threads, and energy-efficient LITTLE cores handle low-intensity software threads that use fewer compute resources. The result is high energy efficiency and high performance. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

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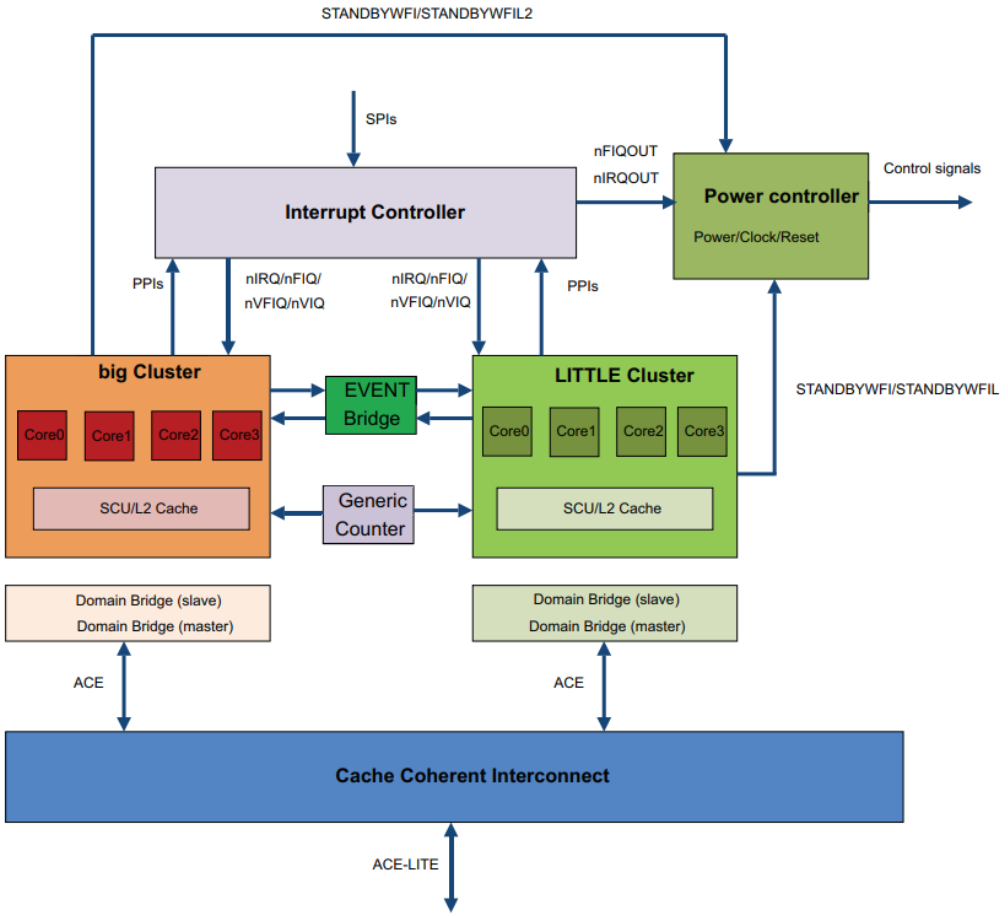
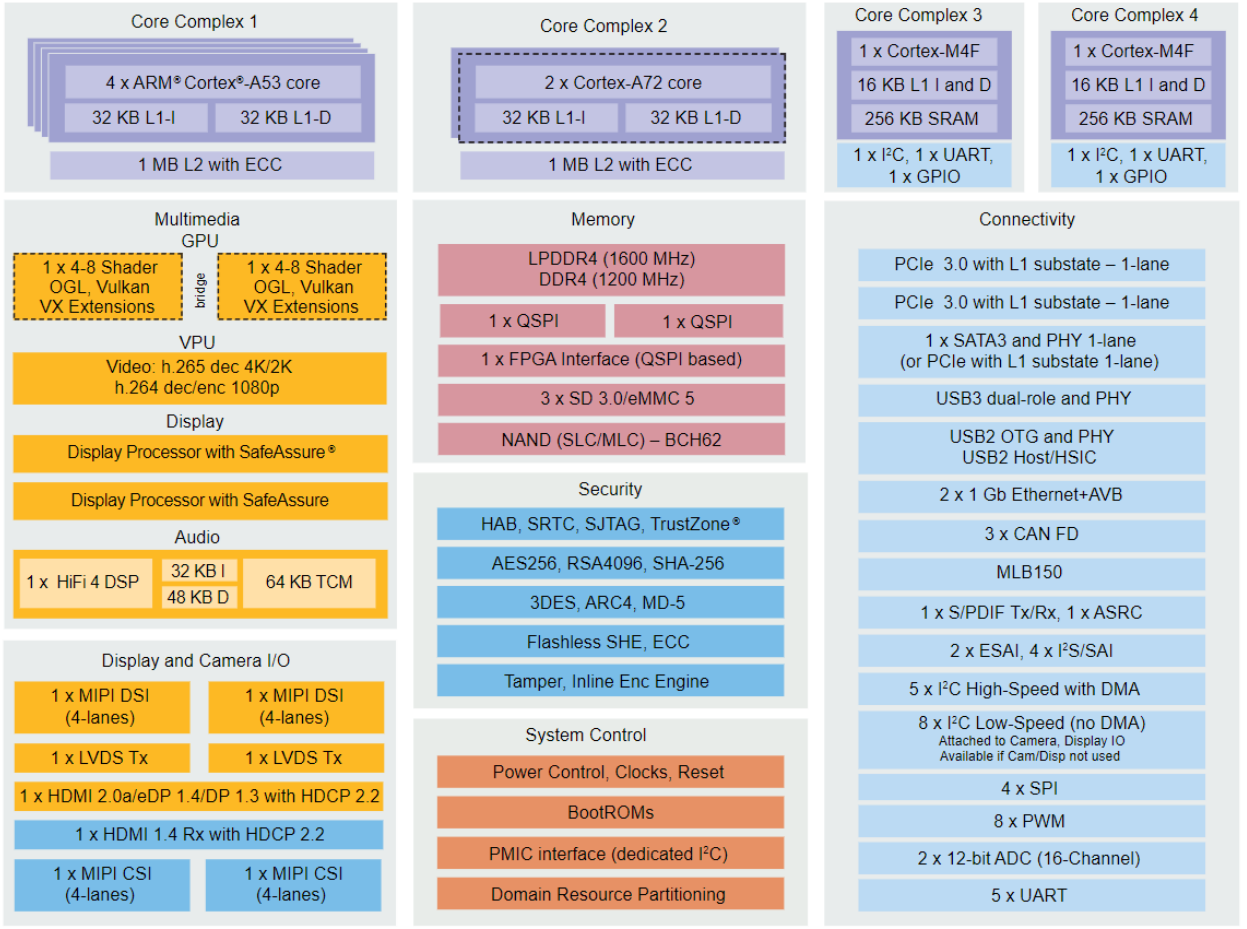
	 **Figure 2-1 A typical big.LITTLE system** "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
[1a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input. For example, the NXP i.MX 8 Family Application Processor includes a first core complex comprising 4 ARM Cortex-A53 cores. The processor cores in the first set receive a dynamic supply voltage and a first output clock signal of a first PLL. ARM documentation for the big.LITTLE architecture used in the i.MX 8 Family Application Processor directly shows that each core cluster (*e.g.*, the Core Complex 1 containing 4 ARM Coretex-A53 cores) receives its own clock domain. At the time the i.MX 8 Family Application Processor was designed, it was typical to produce this clock using a PLL that has a corresponding clock input. Furthermore, ARM documentation for an earlier, related device (the Cortex-A15_A7 MPCore test chip, which also has independent clock domains for different CPU clusters) shows each CPU cluster receiving an output clock signal from a PLL having a corresponding clock signal as input (*e.g.* from an oscillator). It is therefore substantially likely that the i.MX 8 Family Application Processor specifically receives a first output clock signal of a first PLL having a first clock signal as input. *See, e.g.*:

Claim 1	Accused Products



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Claim 1	Accused Products
	Voltage domains The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

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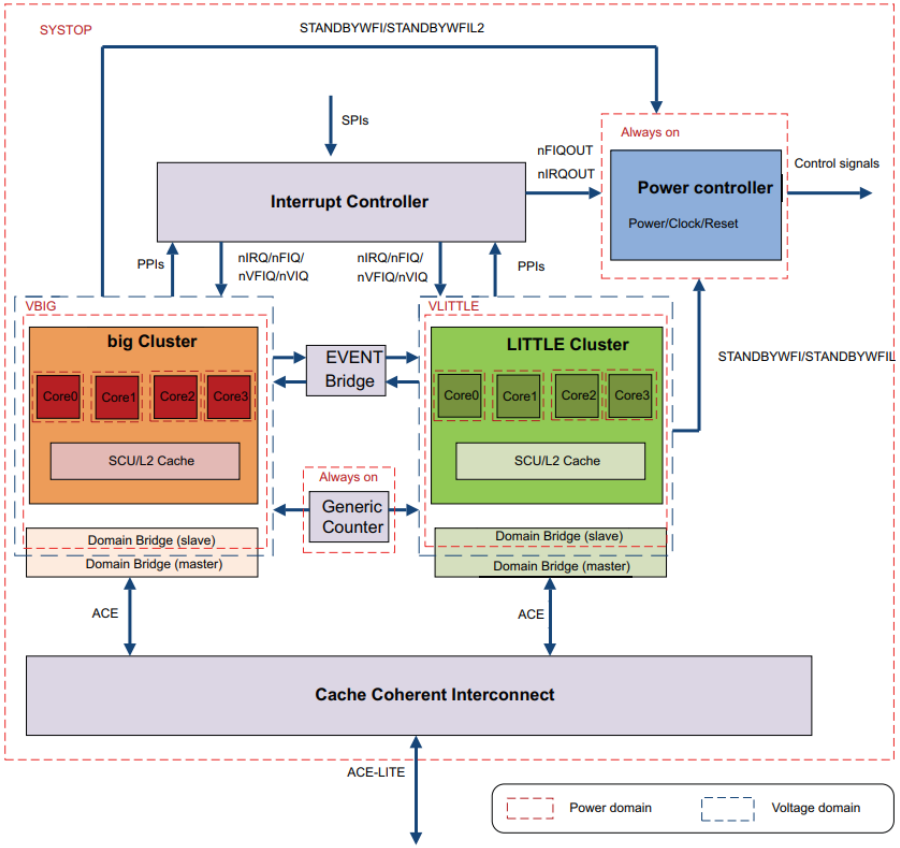

Figure 2-2 Power domain hierarchy

In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP).

"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

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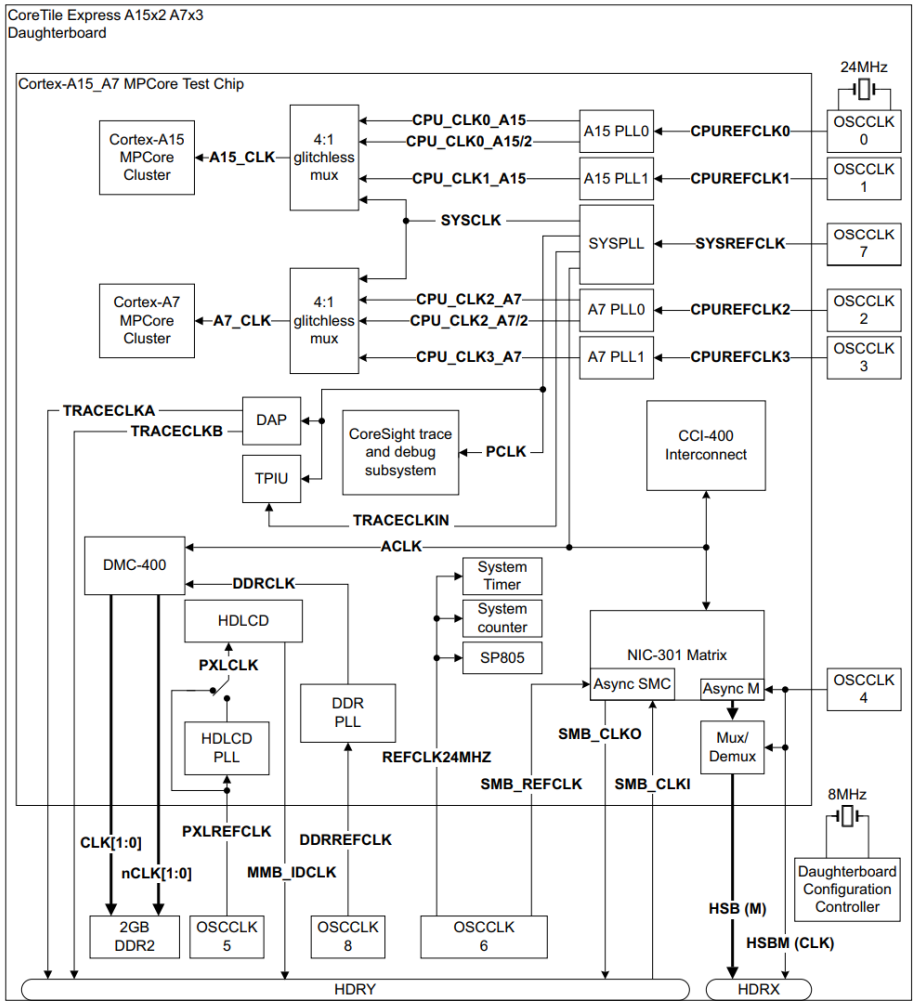

Figure 2-10 CoreTile Express A15×2 A7×3 daughterboard clocks

ARM® CoreTile Express A15×2 A7×3 Technical Reference Manual, available at https://developer.arm.com/documentation/ddi0503/i/

Claim 1	Accused Products
[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal. For example, in addition to the first set of processor cores, the NXP i.MX 8 Family Application Processor includes a second core complex with 2 ARM Cortex-A72 cores. The processor cores in the second set receive a second, independent dynamic supply voltage and a second, independent clock signal of a second PLL. ARM documentation for the big.LITTLE architecture used in the i.MX 8 Family Application Processor directly shows that each core cluster (*e.g.*, the Core Complex 2 containing 2 ARM Coretex-A72 cores) receives its own clock domain. At the time the i.MX 8 Family Application Processor was designed, it was typical to produce this clock using a PLL that has a corresponding clock input. Furthermore, ARM documentation for an earlier, related device (the Cortex-A15_A7 MPCore test chip, which also has independent clock domains for different CPU clusters) shows each CPU cluster receiving an output clock signal from a PLL having a corresponding clock signal as input (*e.g.* from an oscillator). It is therefore substantially likely that the i.MX 8 Family Application Processor specifically receives a first output clock signal of a first PLL having a first clock signal as input. *See, e.g.*:

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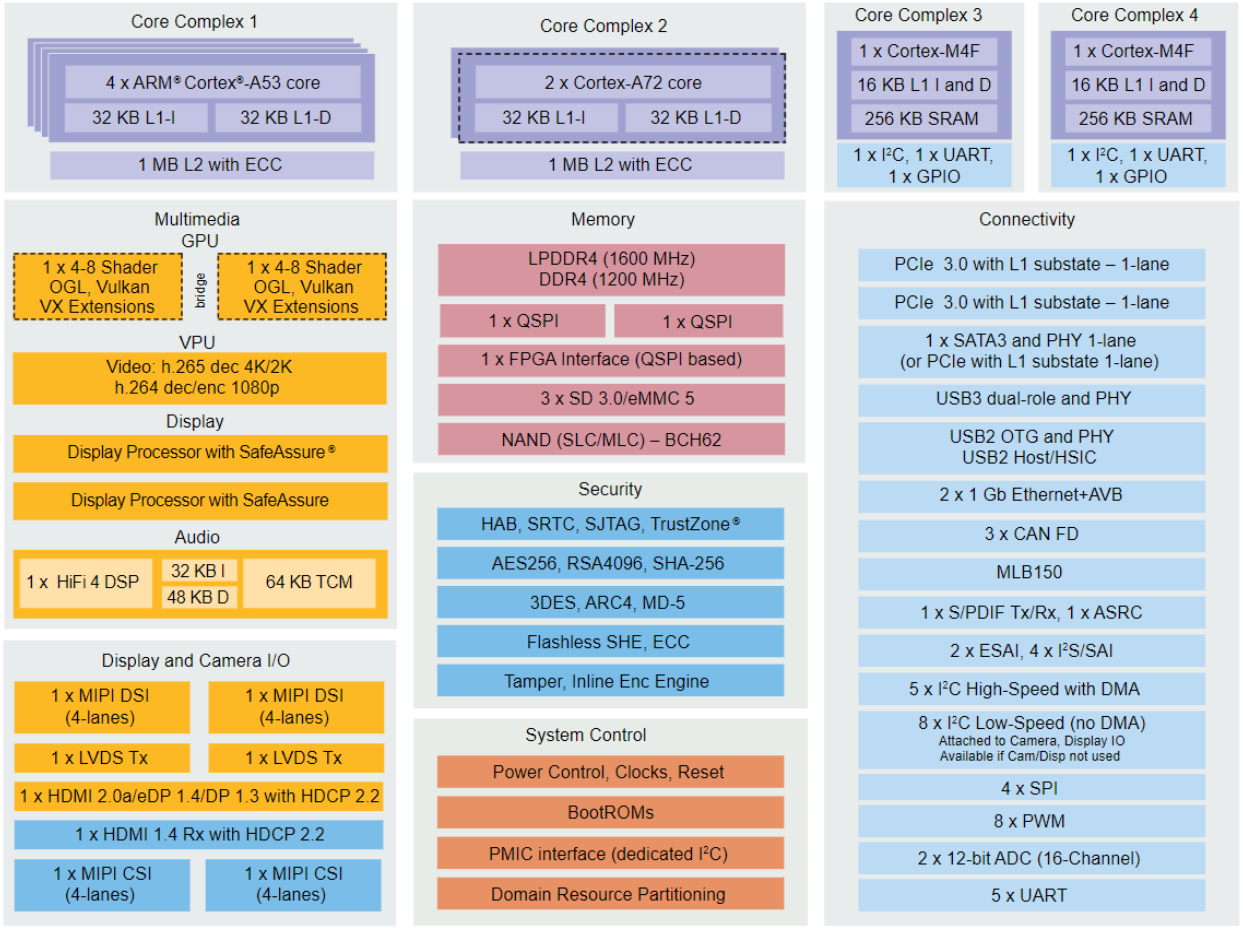

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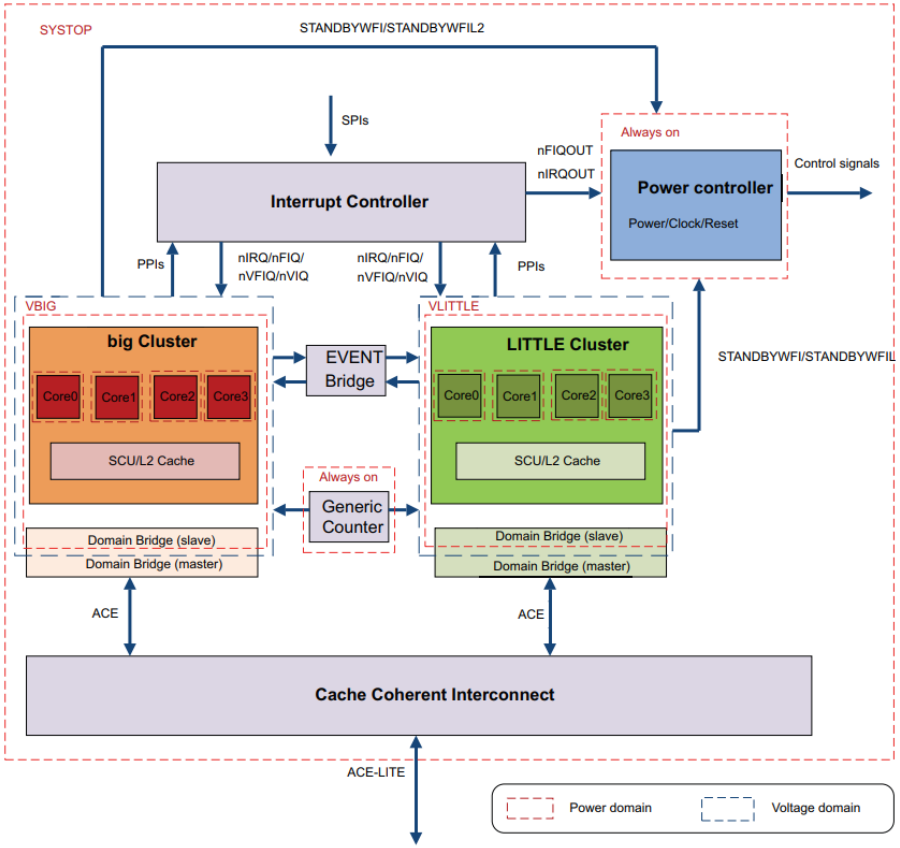

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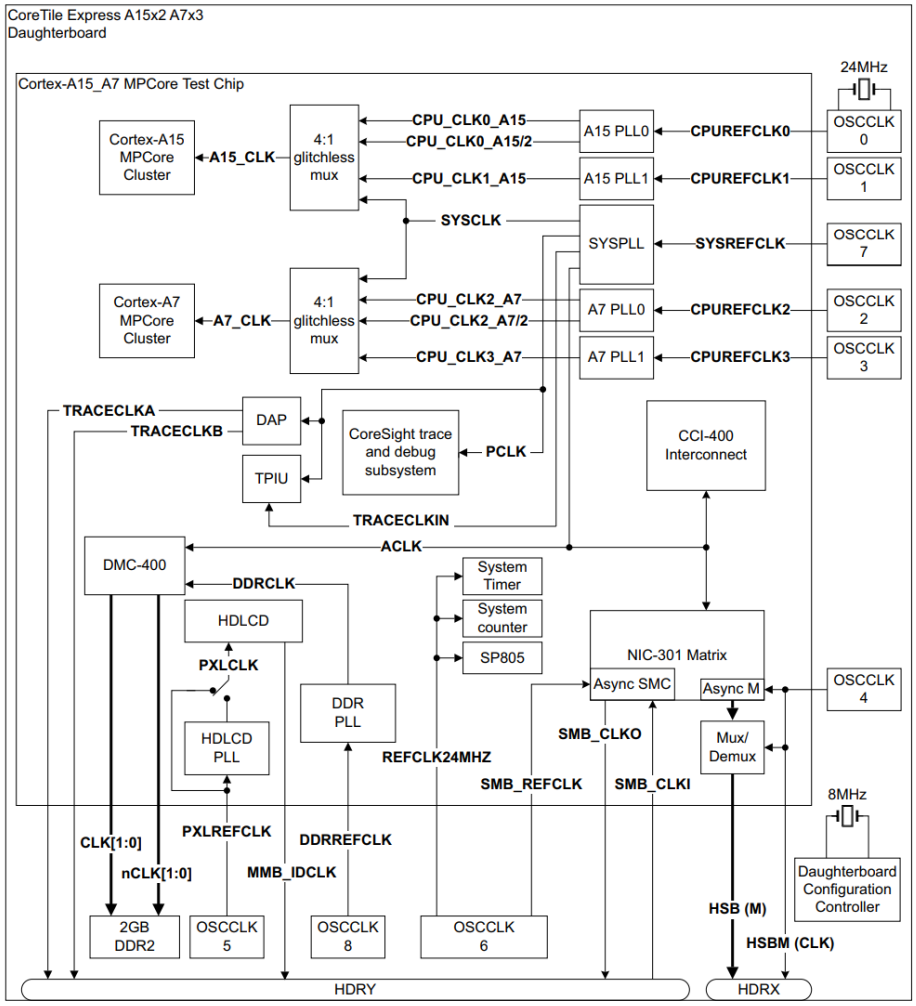

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Claim 1	Accused Products
[1c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. For example, the NXP i.MX 8 Family Application Processor a cache coherent interconnect that is coupled to each core or to each set of processor cores and is configured to maintains coherency between caches in the cores or complexes. As shown in the relevant documentation, described above and reiterated here for the avoidance of all possible doubt, the NXP i.MX 8 Family Application Processor implements the big.LITTLE architecture, which is the heterogeneous processing architecture for the ARM Cortex-A53 and ARM Cortex-A72 processors. The big.LITTLE architecture is also the heterogenous processing architecture for the ARM Cortex-A7 and Cortex-A15 processors. For example, ARM documentation for the big.LITTLE architecture expressly includes all four of these processors in its stated scope. ARM's public documentation of the big.LITTLE architecture describes the infringing cache coherent interconnect in general, and also in the context of a "typical big.LITTLE system" featuring Cortex-A7 and Cortex-A15 processors. There is a reasonable inference that ARM's document also applies to the NXP i.MX 8 Family Application Processor, which includes Cortex-A53 and Cortex-A72 cores. *See, e.g.*:

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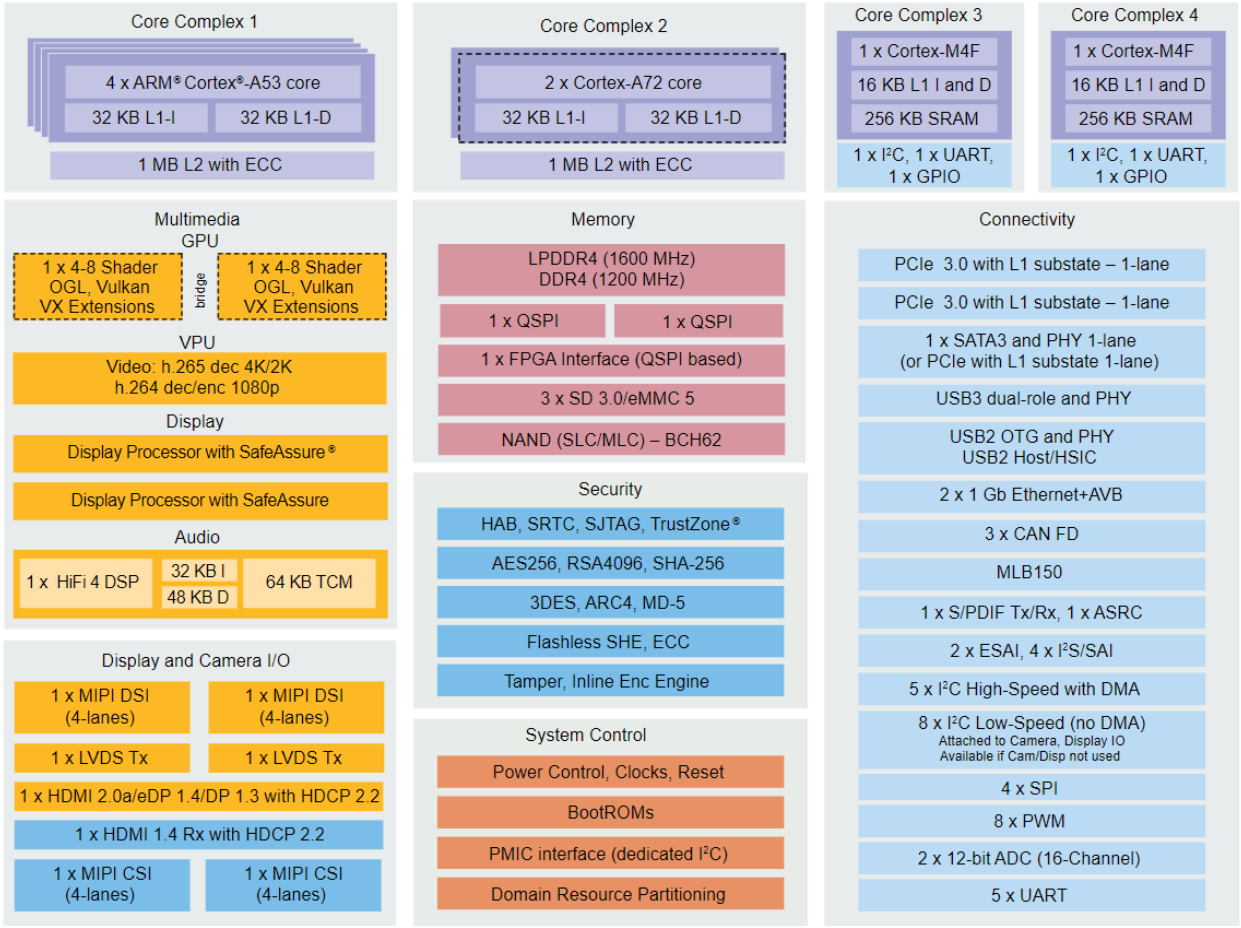

https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-applications-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8

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	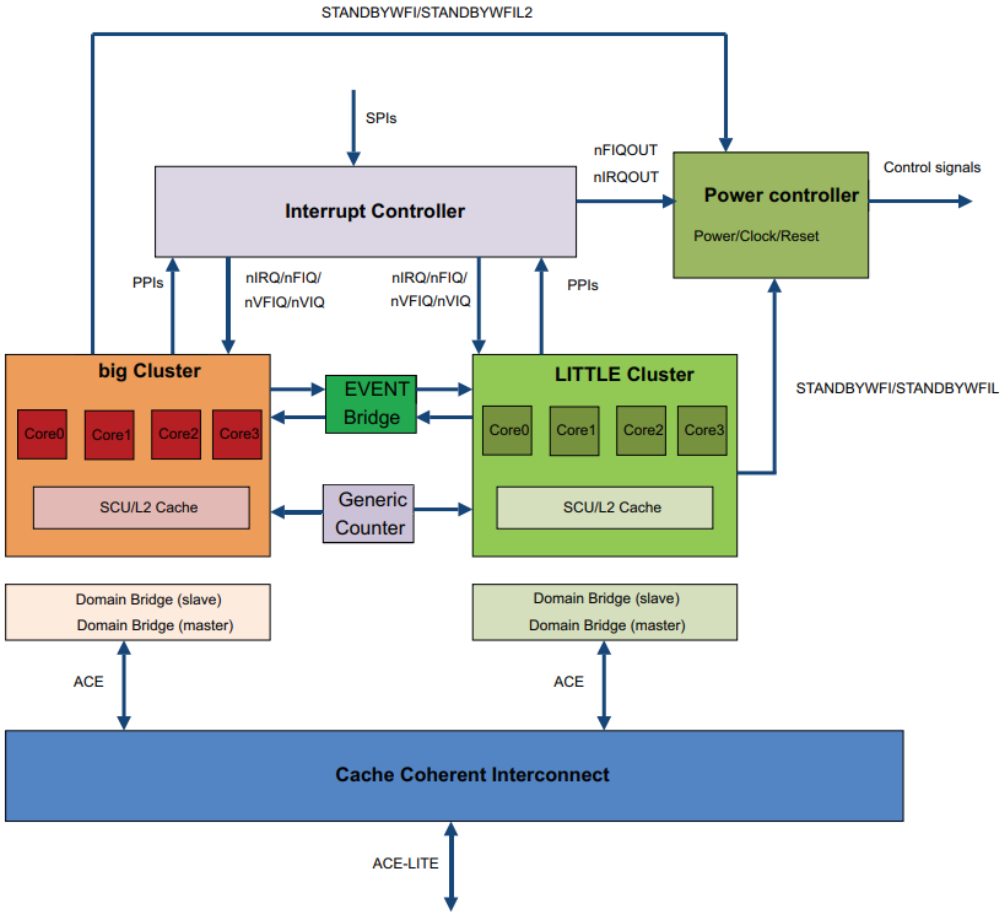 **Figure 2-1 A typical big.LITTLE system** "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

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	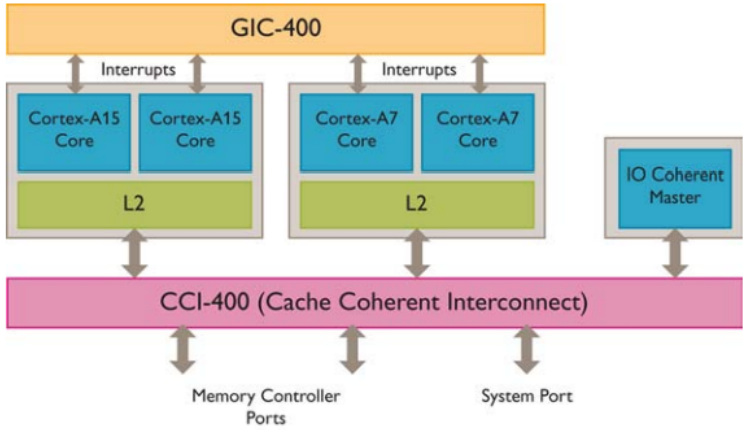 **Fig 1: Typical big.LITTLE system** As an example, Figure 2 describes the pipeline designs for the Cortex-A15 and Cortex-A7 cores. The Cortex-A15 core is designed to achieve high performance by running more instructions in parallel on a bigger and more complex pipeline. On the other hand, the Cortex-A7 core's pipeline is relatively simple and is designed to be extremely power efficient. The Cortex-A7 core's performance is lower than the Cortex-A15 core's but it is sufficient for most common usage scenarios executed by modern mobile devices. In fact, the Cortex-A7 core's performance is close to Cortex-A9 core, which powers most smartphones today. ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

Claim 1	Accused Products
	Cache Coherency Interface and big.LITTLE Technology The key ingredient that makes big.LITTLE technology possible is coherency. big.LITTLE software models require transparent and performant transfer of data between big and LITTLE processors. Hardware coherency enables this, transparently to the software. Without hardware coherency, the transfer of data between big and LITTLE cores would always occur through main memory - this would be slow and not power efficient. In addition, it would require complex cache management software, to enable data conherency between big and LITTLE processors Figure 4 is an example of CPU subsystem consisting of a Cortex-A7 cluster, a Cortex-A15 cluster and a set of system fabric components which enable the seamless data transfer between clusters. This fabric is collectively referred to as a "Cache Coherent Interconnect" – in this case the ARM CoreLink™ CCI-400 interconnect IP. The system is completed by the CoreLink GIC-400, which provides dynamically configurable interrupt distribution to all the cores. ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

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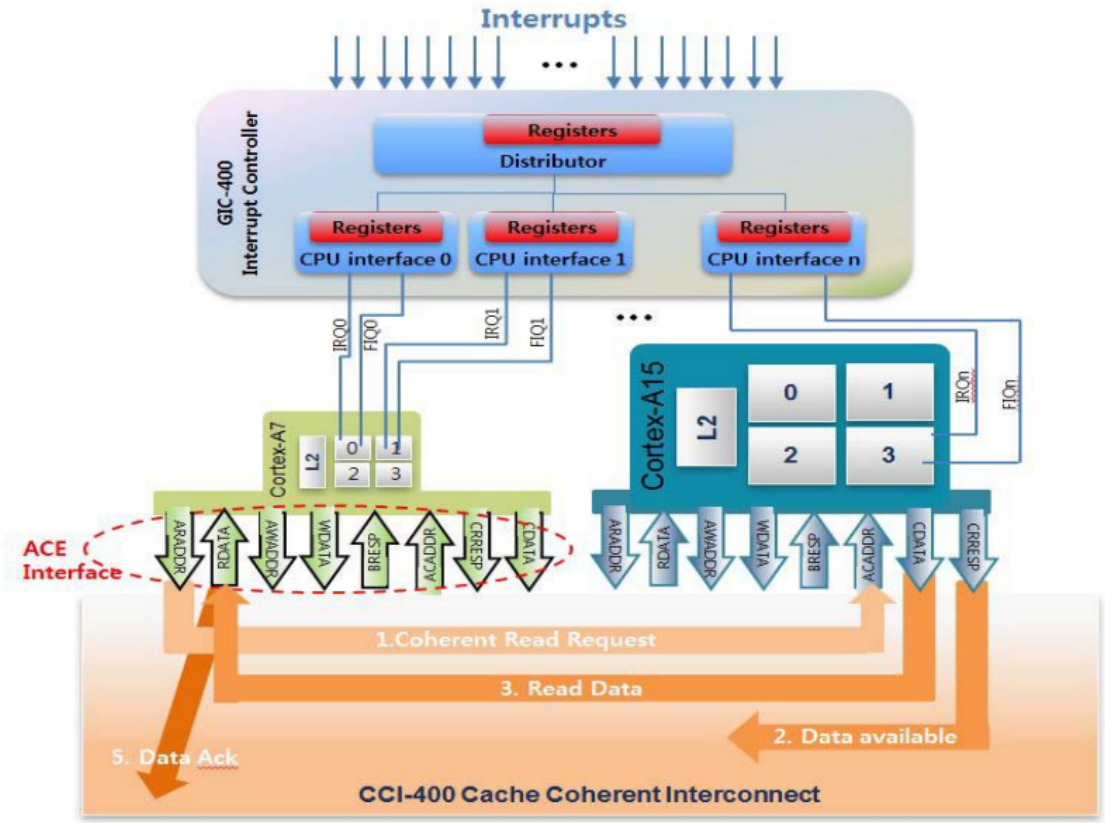

Figure 3: Cache coherency in a big.LITTLE system

ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

Claim 1	Accused Products
	As shown in Figure 3, the bus interfaces of Cortex-A15 and Cortex-A7 processors make use of the AMBA® AXI Coherency Extensions (ACE) to the widely-used AMBA AXI protocol. This protocol provides for coherent data transfer at the bus level. In the AMBA ACE protocol, three coherency channels are added in addition to the normal five channels of AMBA AXI. As an example, the lower part of Figure shows the steps in a coherent data read from the Cortex-A7 cluster to the Cortex-A15 cluster. This starts with the Cortex-A7 cluster issuing a Coherent Read Request through the RADDR channel. The CCI-400 hands over the request to the Cortex-A15 processor's ACADDR channel to snoop into Cortex-A15 processor's cache. On receiving the request from CCI-400, the Cortex-A15 processor checks the data availability and reports this information back through the CRRESP channel. If the requested data is in the cache, the Cortex-A15 processor places it on the CDATA channel. Then the CCI-400 moves the data from the Cortex-A15 processor's CDATA channel to the Cortex-A7 processor's RDATA channel, resulting in a cache linefill in the Cortex-A7 processor. The CCI-400 and the ACE protocol enable full coherency between the Cortex-A15 and Cortex-A7 clusters, allowing data sharing to take place without external memory transactions. ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf